In the Specification

Please substitute the following amended paragraph for the paragraph beginning on page 1, line 16:

Currently, pin functionality is tested by X-ray and [[an]] a pattern estimation program or operator successively. The bus quality test is performed by probing to determine whether two points are active. The connection test, however, is applicable only to circuits and therefore does not yield sufficient data.

Please substitute the following amended paragraph for the paragraph beginning on page 2, line 3:

The method comprises the steps of disposing a first connection circuit on a first programmable array circuit, such as FPGA, according to a preset LFSR polynomial, disposing a second connection circuit on a second programmable array circuit, wherein pins of the second connection circuit are connected to the corresponding pins of the first connection circuit in one-pin-to-one-pin and parallel layout. In one example, one of the two connection circuits has an XOR gate and the other circuit has a shift register. In another example, one circuit has both an XOR gate and a shift register. A pattern is input to the shift register to be processed by the shift register and a specific pattern is produced from an output pin of the shift register is corresponding to the connection status and relevant information about the first and the second connection circuits. The shift register comprises a plurality of D-type flip-flops connected in seriesserial.

Please substitute the following amended paragraph for the paragraph beginning on page 2, line 23:

The test circuit comprises a first connection circuit connected to a first FPGA and a second connection circuit having a shift register and connected between the first connection circuit and a second FPGA, wherein the first and the second connection circuits are disposed according to a preset linear feedback shift register (LFSR) polynomial, wherein a test pattern is input to and processed by the shift register, and then a specific pattern is produced from an output pin of the shift register, and wherein the specific pattern ~~is corresponding~~ corresponds to the connection status of the first and the second connection circuits. The shift register comprises a plurality of D-type flip-flops connected in series ~~serial~~. In this case the first connection circuit has an XOR gate and the second connection circuit has a shift register, and in another case the second connection circuit has both an XOR gate and a shift register.

Please substitute the following amended paragraph for the paragraph beginning on page 4, line 18:

Basically, a unit of an LFSR comprises a plurality of D-type flip-flops and a plurality of XOR gates. The D-type flip-flops are connected in series ~~serial~~ and constitute a shift register. The disposition of the XOR gates determines the characteristic polynomial of the LFSR. The general formula of the structures in FIGS. 1a and 1b can be represented as follow:

$g(x)=g_n x^n+g_{n-1}x^{n-1}+\Lambda+g_0 x^0$.

Please substitute the following amended paragraph for the paragraph beginning on page 5, line 3 (the portion proceeding the formula):

The disposition of the XOR gates determines representation of the characteristic polynomial of the LFSR for any possible form of the characteristic polynomial. A test pattern, for example, "01010001" in FIG. 2b (namely, the pattern is $x+x^3+x^7$), is input to and processed by the shift register. In other words, the test pattern is divided by the characteristic polynomial. If the output pattern is not equal to the predicted pattern, the remainder is indicative of [[,]] an error that has occurred. ~~is happened.~~ By examining the disposition of the XOR gates relating to the output pattern, connection status and relevant information can be acquired. By the recursive feature of the LFSR, the LFSR operates in a fixed sequence, so the output pattern can be acquired and represented as follows:

Please substitute the following amended paragraph for the paragraph beginning on page 6, line 8:

As shown in FIG. 3a, a LFRS polynomial circuit is established by the connections, namely the buses 34, between two FPGAs 31 and 32 to perform the test method. Put simply, using the division feature of the polynomial, after establishing the circuit, a fixed pattern IN is input to the shift register 38 via the input pin 37, and then an output pattern OUT from the output pin 36 is examined. If any of the bus connection lines are connected incorrectly or disconnected, the polynomial formed by the circuit is incomplete and has a corresponding missing term. After inputting a pattern "1111" via the input pin, the pattern OUT is detected as erroneous. Therefore, g(x) is able to be

derived by reversing the formula G(x). If the characteristic polynomial is $g(x)=1+x^2+x^3$ as shown in FIG. 3b and both the polynomial circuit and the input pattern are known, the erroneous connection line relating to the first-order item x is easily detected. Moreover, using a polynomial division operation ~~feature~~, when 0 or 1 is randomly transmitted on the buses 34 and the clock speed varies, the bus speed can be decided according to the corresponding output ~~situation~~. In addition, the appearance of cross talk can be detected upon the occurrence of an incompatible condition gap.